ABSRACT OF THE DISCLOSURE

In a cache memory control method and computer of the present invention, a cache memory is connected to a main memory and divided into a plurality of cache blocks, and a lock/unlock signal is supplied to the cache memory to either set a replace-inhibition state of at least one of the cache blocks in which replacing at least one of the cache blocks to the main memory is inhibited, or reset the replace-inhibition state of at least one of the cache clocks such that replacing at least one of the cache block to the main memory is allowed. Either reading or writing of the main memory is performed by using the remaining cache blocks of the cache memory, other than the at least one of the cache blocks, such that, when the replace-inhibition state is set by the lock/unlock signal, replacing the at least one of the cache blocks to the main memory is inhibited during the reading or writing of the main memory.